THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOON-SUB AUM

Appeal No. 1998-1343
Application No. 08/154,695

ON BRIEF[1]

Before FLEMING, GROSS, and LEVY, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 6, 7, and 9 through 11 (as renumbered by the examiner in the Office action (Paper No. 5) mailed November 21, 1995. Claims 1 through 5 and 8 have been allowed.

[1] We observe that on May 14, 2000 (paper no. 20), appellant filed a waiver of the oral hearing set for May 15, 2000.

Appellant's invention relates to a data processor capable of accessing data stored in a memory which has a data output capacity smaller than the data processing capacity of the central processing unit. Claim 6 is illustrative of the claimed invention, and it reads as follows:

6. A data processor capable of high speed accessing, having a central processing unit for supplying a data output control signal and address signals, comprising:

signal generating means for generating a plurality of storage control signals and first and second address extension signals;

memory means for storing data and sequentially outputting a first portion of said data in response to said address signals and said first address extension signal and a second portion of said data in response to said address signals and said second address extension signals; and

a plurality of register means responsive to said data output control signal and said storage control signals, for receiving said data from said memory means in response to said storage control signals and outputting said data simultaneously in response to said data output control signal.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

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| Diehl | 5,274,786 | Dec. 28, 1993 (filed Nov. 28, 1990) |

Claims 6, 7, and 9 through 11 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Diehl.

Reference is made to the Examiner's Answer (Paper No. 14, mailed February 19, 1997) and the Supplemental Examiner's Answer (Paper No. 18, mailed June 10, 1997) for the examiner's complete reasoning in support of the rejection, and to appellant's Brief (Paper No. 13, filed November 25, 1996), Reply Brief (Paper No. 15, filed April 18, 1997), and Supplemental Reply Brief (Paper No. 19, filed August 11, 1997) for appellant's arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art reference, and the respective positions articulated by appellant and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 6, 7, 10 and 11 and affirm the anticipation rejection of claim 9.

Appellant states (Supplemental Reply Brief, page 4) that "[s]ince several of the arguments traversing the rejection of claim 1 are moot, those arguments now apply to claim 6." Appellant, therefore, requests entry of the Supplemental Reply Brief "to ensure that the issues and arguments are clear." We take this to mean that the arguments formerly directed to the

rejection of claim 1 in the Brief and Reply Brief in addition to arguments set forth in the Supplemental Reply Brief now apply to the rejection of claim 6.

Only two arguments in the Brief and Reply Brief are directed to limitations that appear in the present claims on appeal. First, appellant contends (Brief, pages 4-5 and 9-10, Reply Brief, pages 5-6) that Diehl discloses a data output control signal, OEAB, which is generated by the controller 108, not by the central processing unit (CPU), and that Diehl's CPU does not inherently generate a data output control signal. Appellant's sole argument in the Supplemental Reply Brief repeats and further explains this position (page 5). Accordingly, we will refer primarily to the Supplemental Reply Brief regarding the details of this argument. Second, appellant argues (Brief, pages 5-6, Reply Brief, page 7) that since Diehl does not show the data output control signal, one cannot determine whether the address extension signals (IAddr[2]) alternately have first and second logic states during a generating period of the data output control signal. Arguments that could have been made but were not presented in the briefs are considered waived. See 37 CFR

§ 1.192(a).

"It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim." In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). See also Lindemann Maschinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

> If the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if that element is "inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

In re Robertson, 169 F.3d 743, 49 USPQ2d 1949, 1951 (Fed. Cir. 1999). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Continental Can, 948 F.2d at 1269, 20 USPQ2d at 1749 (quoting In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981).

As to the data output control signal, claims 6, 7, 10, and 11 each require that the CPU generates the signal. Further, the register means (claims 6 and 7) or temporary storage means (claims 10 and 11) outputs data in response to the data output control signal. In Diehl (column 2, lines 9-12), "OEAB enables both lower and upper transceivers 106 and 104 [which the examiner equates to the claimed register or temporary storage means] to drive their contents onto the data bus connecting to microprocessor 100." In other words, signal OEAB has the function of appellant's claimed data output control signal. OEAB, however, is generated by controller 108, not by CPU 100 (see column 2, lines 30-38). Therefore, Diehl does not explicitly disclose the claimed limitation.

The examiner, therefore, resorts to inherency, asserting (Supplemental Answer, page 3) that the CPU inherently generates a data output control signal. The examiner states (id.) that

> [t]he only way controller 108 can know when an i860 read cycle occurs is by some signal (electrical). It is impossible for the controller to know when processor i860 has been instructed to read or write data without receiving some indication. Even if controller 108 were a state machine or processor

> itself it would still have no way of knowing when to perform a memory read or write.

We should note here that the examiner has provided no extrinsic evidence to establish that the CPU necessarily generates a data output control signal, and that it would be so recognized by persons of ordinary skill. See Continental Can, 948 F.2d at 1268, 20 USPQ2d at 1749.

Appellant responds (Supplemental Reply Brief, page 5) to the examiner's assertion as follows:

> There is no reason that the i860 microprocessor can not be controlled by controller 108 instead of controller 108 being controlled by the i860 microprocessor. Accordingly, it is entirely possible that only controller 108 knows when a read from memory is to occur. It is also possible that both the controller and the i860 work in sync with the 33.33 MHZ system clock XClk, wherein a predetermined clock cycle controls whether the i860 microprocessor is in a read or write mode (see for example Diehl's col. 5, line 5 wherein read and write cycles are discussed). Further, there could be some central processing controller not shown which controls both microprocessor 100 and controller 108.

(The above-noted quote is virtually identical to the argument set forth in the Reply Brief at pages 5-6). Thus, appellant has provided several alternatives which indicate that the CPU does not inevitably generate a data output control signal, and

the examiner has shown no reason why the alternatives proposed by appellant are impossible. Further, Diehl's Figure 1 indicates that the CPU actually acts in response to signals generated by controller 108. Accordingly, we find that Diehl's CPU does not inherently generate a data output control signal. Consequently, we cannot sustain the rejection of claims 6, 7, 10, and 11.

Regarding appellant's other argument, each of claims 7, 10, and 11 recites that a signal generating means generates address extension signals have first and second logic states during a generating period of the data output control signal. Appellant contends that since Diehl does not show the data output control signal, one cannot determine whether the address extension signals (IAddr[2]) alternately have first and second logic states during a generating period of the data output control signal. We agree. Therefore, we further reverse the rejection of claims 7, 10, and 11, as Diehl lacks the additional limitation for these claims.

As to claim 9, appellant attempts (Supplemental Reply Brief, page 4) to group claim 9 with claims 6, 7, 10, and 11. Appellant's only argument directed specifically to the

rejection of claim 9 relates to the data output control signal being generated by the CPU (see Brief, page 9). However, no such limitation appears in claim 9. A data output control signal need only be generated, but not by any particular element. Consequently, appellant's argument for claim 9 is not persuasive. Therefore, we will affirm the rejection of claim 9.

## CONCLUSION

The decision of the examiner rejecting claims 6, 7,10, and 11 under 35 U.S.C. § 102(e)is reversed. The decision of the examiner rejecting claim 9 under 35 U.S.C. § 102(e)is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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| MICHAEL R. FLEMING<br>Administrative Patent Judge | ) | |
| ANITA PELLMAN GROSS<br>Administrative Patent Judge | ) | BOARD OF PATENT APPEALS AND INTERFERENCES |
| STUART S. LEVY<br>Administrative Patent Judge | ) | |

ROBERT E. BUSHNELL, ATTORNEY-AT-LAW
1522 K STREET, NW
SUITE 300
WASHINGTON, DC 20005-1202